IN THE CLAIMS:

Claim 1-13 (Canceled)

Claim 14 (New)   A method of manufacturing a semiconductor device comprising:

forming a gate electrode on a semiconductor substrate by performing a lithography process using a reticle, the reticle having a substantially linear gate electrode pattern having paired first and second long sides and a pair of short sides and being set on two transistor regions and sandwiched region between the two transistor regions of the semiconductor substrate, a convex portion in which at least a part of the sandwiched region is arranged being included in the first long side, a concave portion facing at least the entire length of the convex portion being included in the second long side and being substantially in the sandwiched region, a length of the concave portion parallel to the second long side being longer than a length of the convex portion parallel to the first long side, a width of the concave portion parallel to the short side being smaller than a diameter of a contact portion formed in the sandwiched region and on the gate electrode pattern.

Claim 15 (New)   A semiconductor device according to claim 14, wherein the gate electrode pattern corresponds to a gate electrode of a driver transistor of a SRAM memory cell.

Claim 16 (New)   A semiconductor device according to claim 14, wherein the gate electrode pattern corresponds to a gate electrode of a load transistor of a SRAM memory cell.

Claim 17 (New)   A method of manufacturing a semiconductor device comprising:

forming a gate electrode on a semiconductor substrate by performing a lithography process using a reticle, the reticle having an elongative gate electrode pattern and being set on two impurity diffused regions and sandwiched region provided between the two impurity diffused regions of the semiconductor substrate, one side of the gate electrode pattern having a convex portion which is

included in the sandwiched region, an opposite side of the gate electrode pattern having a concave portion which is included substantially in the sandwiched region, a length of the concave portion being longer than a length of the convex portion, a width of the concave portion being smaller than a diameter of a contact portion formed in the sandwiched region and on the gate electrode.

Claim 18 (New)   A method according to claim 17, wherein the gate electrode pattern corresponds to a gate electrode of a drive transistor of a SRAM memory cell.

Claim 19 (New)   A method according to claim 17, wherein the gate electrode pattern corresponds to a gate electrode of a load transistor of a SRAM memory cell.

Claim 20 (New)   A method according to claim 17, wherein the concave portion positionally corresponds to at least a part of the convex portion.

Claim 21 (New)   A method according to claim 17, wherein the concave portion positionally corresponds to an overall of the convex portion.

Claim 22 (New)   A method according to claim 17, wherein the concave portion extends onto gate portions of the impurity diffused regions and positionally corresponds to an overall of the convex portion.